Please amend the subject application as follows:

IN THE CLAIMS:

Claims 1-12 (Canceled)

13. (Original) A method of fabricating a vertical multiple-channel FET device comprising:
providing an integrated circuit substrate;
providing at least two layers of a first composition having a first etch property;
providing at least one layer of a second composition having a second etch property, wherein the at least two layers of the first composition and the at least one layer of the second composition are formed to have a substantially homogenous crystallinity and wherein the at least two layers of the first composition are separated by the at least one layer of the second composition;
forming a blocking layer over the at least two layers of the first composition and the at least one layer of the second composition;
patterning the blocking layer to define placement of a first current electrode region, a second current electrode region and a plurality of channels;
etching exposed portions of the at least two layers of the first composition and the at least one layer of the second composition to form the first current electrode region, the second current electrode region and channel regions extending from the integrated circuit substrate;
further etching the at least one layer of the second composition to remove said at least one layer of the second composition and form the plurality of channels comprised of the first composition and located above and below any removed portion of the at least one layer of the second composition;
depositing a control electrode dielectric around each of the plurality of channels;
depositing control electrode material around the control electrode dielectric;
selectively masking and etching the control electrode material to form a control electrode on top, bottom and sidewall surfaces of at least one of the plurality of channels; and

forming a spacer to isolate the control electrode material from the first current electrode region and the second current electrode region.

14. (Original) The method of claim 13 wherein providing the at least two layers of a first composition having a first etch property comprises forming the at least two layers of the first composition by epitaxially growing the at least two layers of the first composition.

15. (Original) The method of claim 13 further comprising:
forming additional material overlying areas adjacent the control electrode and the spacer to reduce resistance of the first current electrode region and the second current electrode region of the vertical multiple-channel FET device.

16. (Original) The method of claim 13 further comprising:
etching the at least one layer of the second composition at the first current electrode region and the second current electrode region; and
forming additional material at areas not covered by the control electrode and the spacer to reduce resistance of the first current electrode region and the second current electrode region of the vertical multiple-channel FET device.

17. (Original) The method of claim 13 further comprising selecting composition of the integrated circuit substrate to be one of the group consisting of silicon, silicon on insulator, silicon on sapphire, and silicon on nitride.

18. (Original) The method of claim 13 further comprising forming the integrated circuit substrate as a plurality of layers, one of the plurality of layers of the integrated circuit substrate having the first composition.

19. (Original) The method of claim 13 further comprising providing the integrated circuit substrate as a silicon-on-insulator (SOI) bonded wafer having a silicon layer which functions as one of the at least two layers of the first composition.

20. (Original) The method of claim 13 further comprising providing the at least two layers of a first composition and the at least one layer of a second composition by using at least one of the group of processes consisting of epitaxial growth, atomic layer deposition, and molecular beam epitaxy.

21. (Original) The method of claim 13 further comprising selecting the first composition from one of the group consisting of silicon, germanium, silicon germanium and silicon germanium carbon and selecting the second composition from one of silicon, germanium, silicon germanium and silicon germanium carbon.

22. (Original) The method of claim 13 further comprising selecting the first composition from one of the group consisting of gallium arsenide, gallium nitride and indium phosphide, and selecting the second composition from one of the group consisting of gallium arsenide, gallium nitride and indium phosphide.

23. (Original) The method of claim 13 further comprising forming the blocking layer from one of the group consisting of photoresist, nitride, oxide, and organic anti-reflective coating.

24. (Original) The method of claim 13 wherein the further etching of the at least one layer of the second composition to remove said at least one layer of the second composition and form the plurality of channels further comprises etching to create a height of each of the plurality of channels to be less than a length of the control electrode.

25. (Original) The method of claim 13 further comprising:

blocking the control electrode by using a blocking layer before etching the at least one layer of the second composition to remove the at least one layer of the second composition at least at the plurality of channels.